

REMARKS

In response to the Office Action, Applicant respectfully requests the Examiner to reconsider the above-captioned application in view of the foregoing amendments and the following comments.

Discussion of Claim Rejections Under 35 U.S.C. § 102(e) and 103(a)

Applicant has the following comment with respect to the Examiner's rejections under 35 U.S.C. §§ 102(e) and 103(a).

Claims 1, 4, and 10

In the Office Action, the Examiner rejected Claims 1, 4, and 10 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,260,892 to Testa (hereinafter "Testa"). One embodiment of Applicant's invention includes a switch that is used to control the parasitic capacitance of a bus. Furthermore, the switch is integrated with a memory circuit. Claim 1 recites: "a switch for decoupling said data bus from said memory circuit when no memory access is being requested by said memory controller so as to reduce parasitic capacitance of said data bus, wherein the switch is an integrated part of the memory circuit." Independent Claims 4 and 10 recite similar limitations.

Applicant respectfully submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *See* M.P.E.P. § 2131. Applicant respectfully submits that Testa fails to teach or suggest at least one limitation from each of independent Claims 1, 4, 7 and 10.

Testa describes a driver (26). The driver (26) routes signals from a memory controller (8) to DRAM chips (27). *See* Testa, col. 5, lines 50-51. Testa teaches positioning the driver (26) such that the trace length to each of the DRAM chips is minimized thereby decreasing the trace capacitance. Applicant respectfully submits that there is no teaching or suggestion in Testa that the driver (26) is used in operation to control the parasitic capacitance of the bus. The driver (26) merely acts as a router of information. It does not control parasitic capacitance, such as by example, electrically isolating via a switch portions of proximately positioned lines in a bus.

Furthermore, Testa fails to teach or suggest a use of a switch that is integrated part of a memory circuit. Assuming for purposes of argument that the driver (26) corresponds to the

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switch as claimed, Testa fails to teach or suggest that the driver (26) be an integrated part of the RAM (26).

Since Testa fails to teach or suggest at least the above limitations, Applicant respectfully submits that independent Claims 1, 4 and 10 are in condition for allowance.

Claims 2, 3, 5, 6, 11, and 12

Claims 2, 3, 5, 6, 11 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Testa in view of U.S. Patent No. 6,011,710, to Wiggers (hereinafter "Wiggers"). Since Claims 2, 3, 5, 6, 11 and 12, each depend on one claims 1, 4 and 10 Applicant respectfully submits that these claims are allowable for the reasons discussed above.

Summary

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. Accordingly, amendments to the claims for patentability purposes, the reasons therefore, and arguments in support of the patentability of the pending claim set are presented above. Any claim amendments which are not specifically discussed in the above remarks are not made for patentability purposes, and the claims would satisfy the statutory requirements for patentability without the entry of such amendments. In addition, such amendments do not narrow the scope of the claims. Rather, these amendments have only been made to increase claim readability, to improve grammar, and to reduce the time and effort required of those in the art to clearly understand the scope of the claim language. In light of the above amendments and remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested. If the Examiner has any questions which may be answered by telephone, he is invited to call the undersigned directly.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

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By: E. M. Nelson
Eric M. Nelson
Registration No. 43,829
Attorney of Record
Customer No. 20,995
(619) 235-8550